CLAIMS:

1. In a capacitor-over-bit line memory array, a method of forming a conductive capacitor plug comprising extending conductive material from proximate a substrate node location to a location elevationally above all conductive material of an adjacent bit line.

2. The method of claim 1, wherein the extending comprises etching a contact opening through insulative material after forming said bit line and forming conductive material within the contact opening.

3. The method of claim 2, wherein the forming of the conductive material comprises forming a storage capacitor at least partially within the contact opening.

4. The method of claim 1, wherein the extending comprises etching a contact opening through two separately-formed insulative material layers, at least a portion of the contact opening being generally self-aligned to said bit line, and forming conductive material within the contact opening.

5. The method of claim 1, wherein the array comprises a word line elevationally below the bit line, and the extending comprises etching a contact opening through insulative material and generally self-aligned to both said bit line and said word line.

6. The method of claim 5, wherein the insulative material comprises two or more separately-formed insulative material layers.

7. The method of claim 1, wherein the extending comprises:

forming a patterned masking layer over the substrate and defining an opening pattern over said substrate node location;

etching insulative material through the opening pattern sufficient to form a contact opening after forming said bit line; and

forming conductive material within the contact opening.

8. The method of claim 7, wherein said opening pattern is formed over a plurality of substrate node locations over which individual capacitors are to be formed.

9. The method of claim 1, wherein said substrate node location comprises a diffusion region, and the extending comprises:

etching a contact opening through insulative material to substantially expose a portion of the diffusion region after forming said bit line; and

forming conductive material within the contact opening and in electrical communication with the diffusion region.

10. The method of claim 9, wherein said insulative material comprises two separately-formed layers of insulative material.

11. In a capacitor-over-bit line memory array, a method of forming a capacitor contact opening comprising etching an opening through a first insulative material received over a bit line and a word line substantially selective relative to second insulative material covering the bit line and the word line to a substrate location proximate the word line in a self-aligning manner relative to both the bit line and the word line.

12. The method of claim 11, wherein the first insulative material comprises separately-formed layers of insulative material.

13. The method of claim 11, wherein the first insulative material comprises two separately-formed layers of insulative material.

14. The method of claim 11, wherein the second insulative material separately encapsulates the bit line and the word line.

15. The method of claim 11, wherein the substrate location comprises a diffusion region, and the etching comprises outwardly exposing the diffusion region.

16. The method of claim 11, wherein the etching comprises removing all of the first insulative material from over the bit line.

17. The method of claim 11, wherein the etching comprises forming a patterned masking layer over the first insulative material defining an opening pattern, and etching the opening through the opening pattern.

18. The method of claim 11 further comprising forming conductive material within the opening, the conductive material extending to an elevation laterally proximate conductive portions of the bit line.

19. The method of claim 11 further comprising forming conductive material within the opening, the conductive material extending to a location elevationally higher than any conductive portion of the bit line.

20. In a capacitor-over-bit line memory array, etching an array of capacitor contact openings to elevationally below the bit lines after forming the bit lines.

21. The method of claim 20, wherein the etching comprises etching openings down to proximate individual substrate diffusion regions.

22. The method of claim 20, wherein the etching comprises etching openings down to proximate individual word lines of the array.

23. The method of claim 22, wherein the etching comprises exposing individual substrate diffusion regions intermediate the word lines.

24. The method of claim 20, wherein etching comprises selectively etching through first insulative material relative to second insulative material covering portions of the bit lines.

25. The method of claim 20, wherein the etching comprises selectively etching through first insulative material relative to second insulative material covering portions of the bit lines and word lines of the array.

26. The method of claim 25, wherein the first insulative material comprises a plurality of separately formed layers of first insulative material.

27. The method of claim 20 further comprising forming conductive material within the contact openings, the conductive material extending to at least laterally proximate conductive portions of the bit lines.

28. The method of claim 20 further comprising forming conductive material within the contact openings, the conductive material extending elevationally higher than any conductive portions of the bit lines.

29. A method of forming a capacitor-over-bit line memory array comprising:

forming a plurality of word lines over a substrate, the word lines having insulating material thereover;

forming a plurality of bit lines over the word lines, the bit lines having insulating material thereover;

forming insulative material over the word lines and the bit lines, the insulative material being etchably different from the insulating material over the word lines and the insulating material over the bit lines; and

selectively etching capacitor contact openings through the insulative material relative to the insulating material over the bit lines and the insulating material over the word lines, the openings being self-aligned to both bit lines and word lines and extending to proximate the substrate.

30. The method of claim 29, wherein the forming of the insulative material comprises forming a plurality of layers of insulative over at least one of the word lines and bit lines.

31. The method of claim 29, wherein forming of the insulative material comprises forming one layer of insulative material over the word lines, and after the forming of the bit lines, forming another layer of insulative material over the bit lines.

32. The method of claim 31 further comprising forming a patterned masking layer over the insulative material defining a mask opening, the mask opening being received over a plurality of substrate locations over which the capacitor contact openings are to be etched, and the etching of the capacitor contact openings comprises etching said contact openings through said mask opening.

33. The method of claim 29 further comprising forming conductive material within the contact openings, the conductive material being formed to extend from proximate individual substrate diffusion regions to at least locations which are elevationally coincident with conductive material of the individual bit lines.

34. The method of claim 29 further comprising forming conductive material within the contact openings, the conductive material being formed to extend from proximate individual substrate diffusion regions to locations elevationally higher than any conductive material of any of the bit lines.

35. A method of forming a capacitor-over-bit line memory array comprising:

forming a plurality of word lines over a substrate;

forming a plurality of bit lines over the word lines;

forming insulative material over the word lines and the bit lines; and

after forming the bit lines, etching an opening through the insulative material and outwardly exposing a diffusion region received within the substrate proximate a word line.

36. The method of claim 35, wherein the forming of the insulative material comprises forming two separate layers of insulative material over the substrate, and the etching of the opening comprises etching the two layers selectively relative to insulative coverings formed over portions of both the bit lines and the word lines.

37. The method of claim 35 further comprising forming conductive material within the opening, the conductive material extending from proximate the diffusion region to a location elevationally higher than any conductive material of the bit lines.

38. A method of forming a memory array comprising in sequence:

forming a plurality of conductive lines over a substrate;

forming a conductive bit line plug intermediate a pair of the conductive lines;

forming a bit line in electrical communication with the conductive bit line plug;

forming a conductive capacitor plug proximate one of the pair of conductive lines, which capacitor plug extends away from the substrate and terminates above conductive portions of the bit line; and

forming a capacitor over and in electrical communication with the capacitor plug.

39. The method of claim 38, wherein the memory array is a capacitor-over-bit line memory array.

40. The method of claim 38, wherein the bit line plug and bit line comprise at least one common material.

41. The method of claim 38, wherein the bit line plug and bit line comprise at least one common material, said common material being deposited in a common processing step.

42. The method of claim 38, wherein the forming of the capacitor plug comprises forming said surface elevationally higher than any conductive portion of the bit line.

43. The method of claim 38 further comprising prior to the forming of the conductive bit line plug, forming first insulative material over the conductive lines, and wherein the forming of the conductive capacitor plug comprises substantially selectively etching an opening into the first insulative material relative to second insulative material over the conductive lines.

44. The method of claim 38 further comprising prior to the forming of the conductive capacitor plug, forming first insulative material over the bit line, and wherein the forming of the conductive capacitor plug comprises substantially selectively etching an opening into the first insulative material relative to second insulative material over the bit line.

45. The method of claim 38 further comprising:

prior to the forming of the conductive bit line plug, forming a first layer of first insulative material over the conductive lines; and

prior to the forming of the conductive capacitor plug, forming a second layer of first insulative material over the bit line,

wherein the forming of the conductive capacitor plug comprises substantially selectively etching an opening into the first insulative material relative to second insulative material over the conductive lines and bit line.

46. The method of claim 45, wherein the etching comprises exposing a substrate diffusion region proximate the conductive lines.

47. A method of forming a memory array comprising:

forming a plurality of word lines over a substrate, the word lines being encapsulated with a first insulative material;

forming a second layer of a second insulative material over the word lines, the second insulative material having a generally planar uppermost surface;

patterning the layer of second insulative material to define a bit line plug opening exposing a first substrate diffusion region between two of the word lines;

forming conductive material over at least a portion of said second insulative material and in electrical communication with the first substrate diffusion region;

removing some of the conductive material over the substrate diffusion region to form a bit line plug in said opening;

forming a bit line over the second insulative material and in electrical communication with the bit line plug, the bit line being encapsulated with a third insulative material;

forming a layer of a fourth insulative material over the bit line;

patterning the layer of fourth insulative material to define an opening over a second substrate diffusion region, said second substrate diffusion region being on an opposite side of one of two word lines between which the bit line plug was formed to form an opening which is generally self-aligned to both the word lines and the bit line; and

forming conductive material within said self-aligned opening and extending to a location higher than the bit line.

48. A method of forming a memory array comprising:

forming a plurality of word lines over a substrate, the word lines having insulating material thereover;

forming a plurality of bit lines over the word lines, the bit lines having insulating material thereover;

forming insulative material over the word lines and the bit lines, the insulative material being etchably different from the insulating material over the word lines and the insulating material over the bit lines; and

selectively etching contact openings through the insulative material relative to the insulating material over the bit lines and the insulating material over the word lines, the openings being self-aligned to both bit lines and word lines and extending to proximate the substrate.